

1 WHAT IS CLAIMED IS

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1. A semiconductor device, comprising:
a Si substrate; and
a resistance element formed on said Si
substrate,

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said resistance pattern) comprising:

a first resistance pattern provided on said
substrate at a first level; and

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a second resistance pattern provided adjacent
to said second resistance pattern) at a second level
lower than said first level, said second resistance
pattern being connected in series to said first
resistance pattern,

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said second resistance pattern having an edge
defined by said first resistance pattern.

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2. A semiconductor device as claimed in claim
1, wherein said resistance element further includes an

1 interlayer insulation pattern underneath said first
resistance pattern with a shape in conformity with a
shape of said first resistance pattern, said second
resistance pattern being provided at a level lower than
5 said interlayer insulation pattern.

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10 3. A semiconductor device as claimed in claim
1, wherein said first resistance pattern includes a
polysilicon pattern and a polycide region formed on said
polysilicon pattern, said semiconductor device further
comprising a MOS transistor having a polysilicon gate
15 electrode having a composition substantially identical
with a composition of said polysilicon pattern.

20 4. A semiconductor device as claimed in claim
1, wherein said first resistance pattern and said second
resistance pattern have a substantially identical
resistance.

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1 5. A semiconductor device as claimed in claim
3, wherein said second resistance pattern is formed in
said Si substrate in the form of a salicide region
defined by said first resistance pattern.

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10 6. A semiconductor device as claimed in claim
5, wherein said Si substrate includes an impurity
element with a concentration level such that a parasitic
MOS transistor, formed of said first resistance pattern
acting as a gate electrode and a pair of said second
resistance patterns at both lateral side of said first
15 resistance pattern acting as source and drain regions,
has a threshold voltage larger than a supply voltage
used in said semiconductor device.

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25 7. A semiconductor device as claimed in claim
1, wherein said second resistance pattern is formed on a
device isolation film covering said substrate, said
second resistance pattern including a first polysilicon

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1 pattern provided on said insulation film and a salicide
region formed on a surface part of said first
polysilicon pattern defined by said first resistance
pattern.

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8. A semiconductor device as claimed in claim
10 7, wherein said first resistance pattern includes a
second polysilicon pattern and a polycide region formed
on said second polysilicon pattern, said second
polysilicon pattern having an impurity concentration
level substantially larger than an impurity
15 concentration level of said first polysilicon pattern.

20 9. A method of fabricating a semiconductor
device, comprising the steps of:
forming a conductive layer on a Si layer;
patterning said conductive layer selectively
with respect to said Si layer, to form a conductor
25 pattern;

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1 depositing a metal film on said Si layer such
that said conductive film covers said conductor pattern
and an exposed part of said Si layer exposed by said
conductive film;

5 annealing said metal film to form a salicide
pattern in correspondence to said conductive pattern as
a first resistance pattern, said annealing step further
forming a salicide pattern in said Si layer in
correspondence to said exposed part of said Si layer as
10 a second resistance pattern; and

 forming a conductor pattern connecting said
first resistance pattern and said second resistance
pattern in series.

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